said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.--

Please replace claim 4 with the following (a marked up version is in the Appendix):

--4.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.--

Please replace claim 15 with the following (a marked up version is in the Appendix):

--15.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

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forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric; and

forming a non-insulating layer over at least a portion of the resultant structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.--

Please replace claim 26 with the following (a marked up version is in the Appendix):

--26.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.--

Please replace claim 33 with the following (a marked up version is in the Appendix):

--33.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

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forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å; and

forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.--

Please replace claim 36 with the following (a marked up version is in the Appendix):

--36.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the structure resultant from said forming a conformal layer;

forming a patterned mask over the structure resultant from said forming an ARL; and

etching said conductive layer using said patterned mask.--

Please replace claim 40 with the following (a marked up version is in the Appendix):

--40.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

providing a process flow for etching said conductive layer, whereby the gates of one or more transistors are formed, said flow including a photolithographic process comprising:

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conductive layer; and

forming a patterned mask over said ARL, wherein said photolithographic process is optimized for forming said gates;

performing a capacitor formation process comprising:

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forming one or more capacitor structures, each comprising a top electrode over a portion of said conductive layer and a dielectric layer between the top electrode and the conductive layer; and

forming a conformal insulating layer over said capacitor structures and at least a portion of said conductive layer proximate to capacitor structures, wherein the capacitor formation process is performed prior to forming said ARL, whereby said ARL is additionally formed over said capacitor structures, and whereby said conformal insulating layer is formed such that said provided process flow is unaltered; and

etching said conductive layer according to said process flow, whereby the lower electrodes of said capacitor structures and said gates are formed.--

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